

FIG. 1

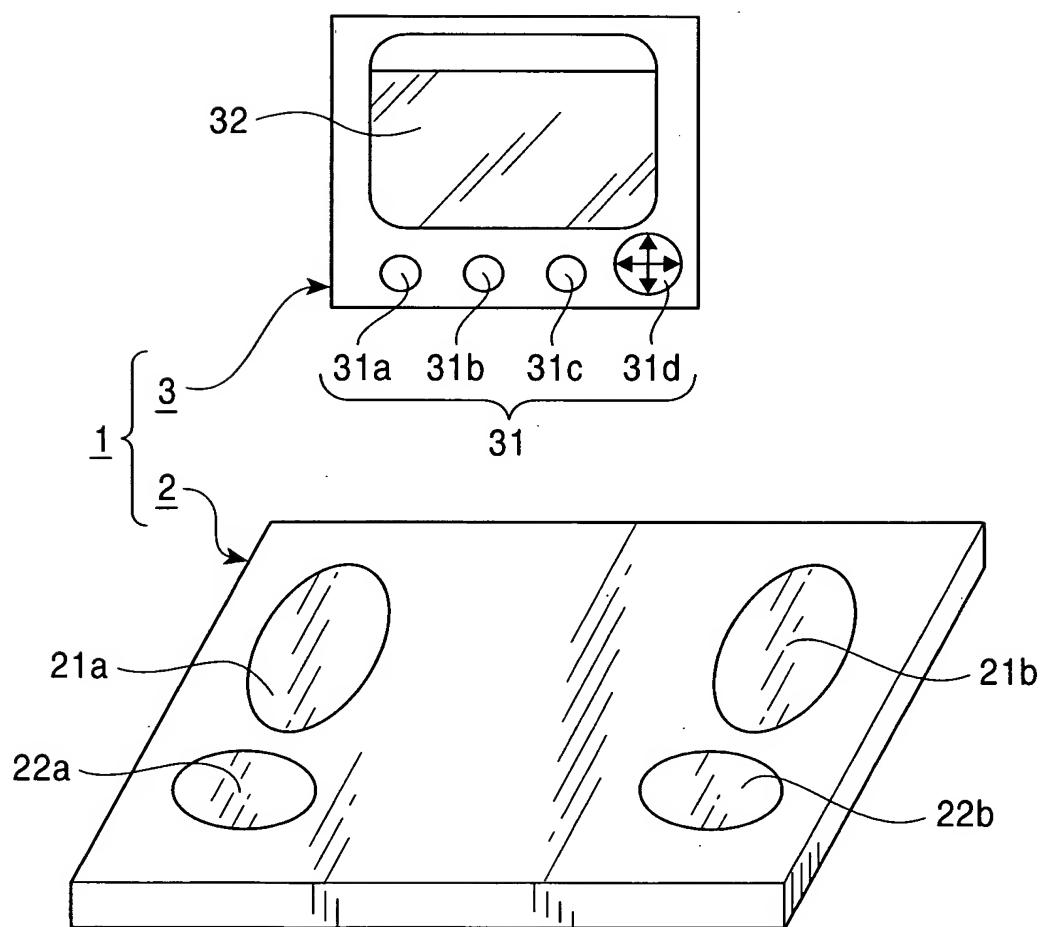


FIG. 2

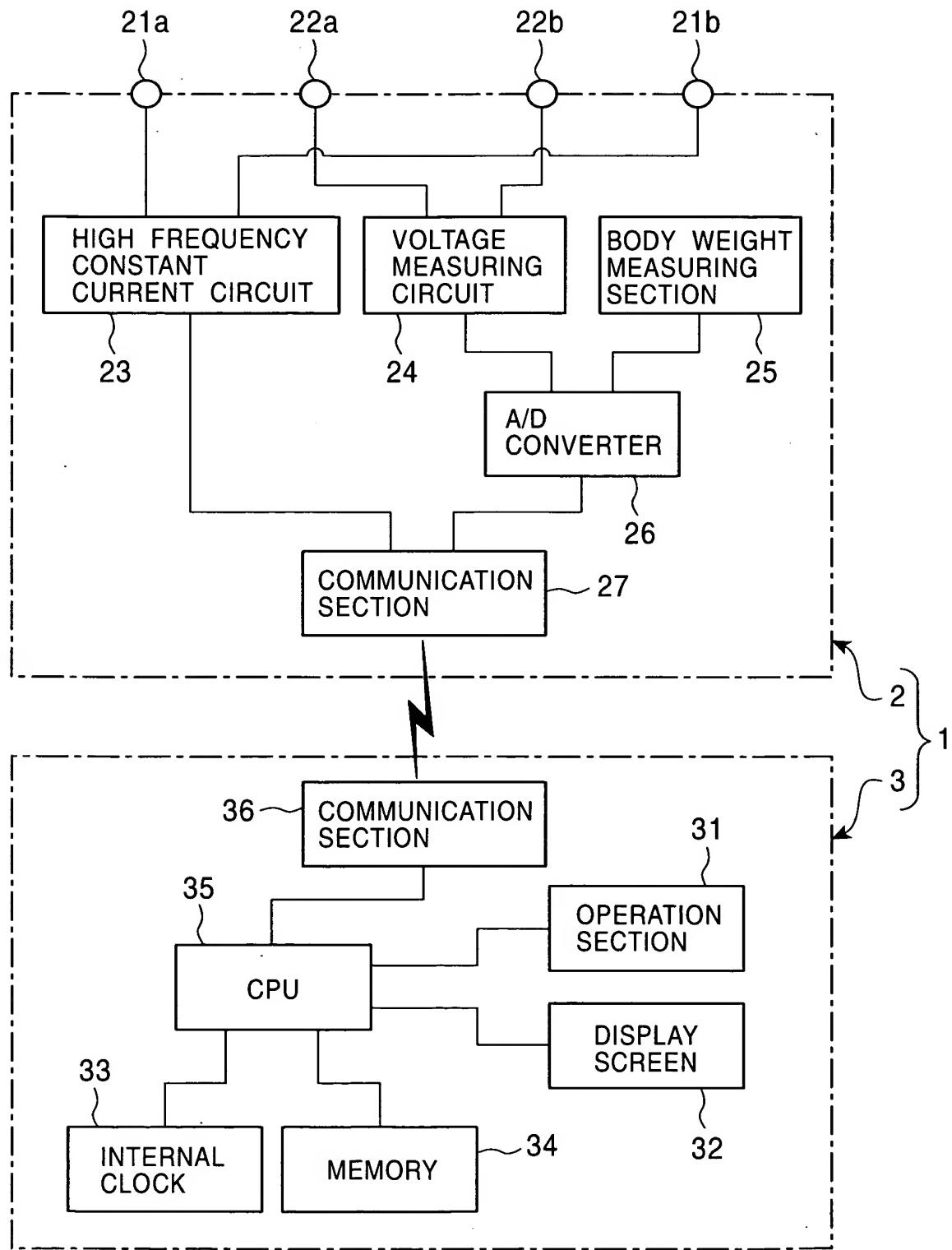


FIG. 3

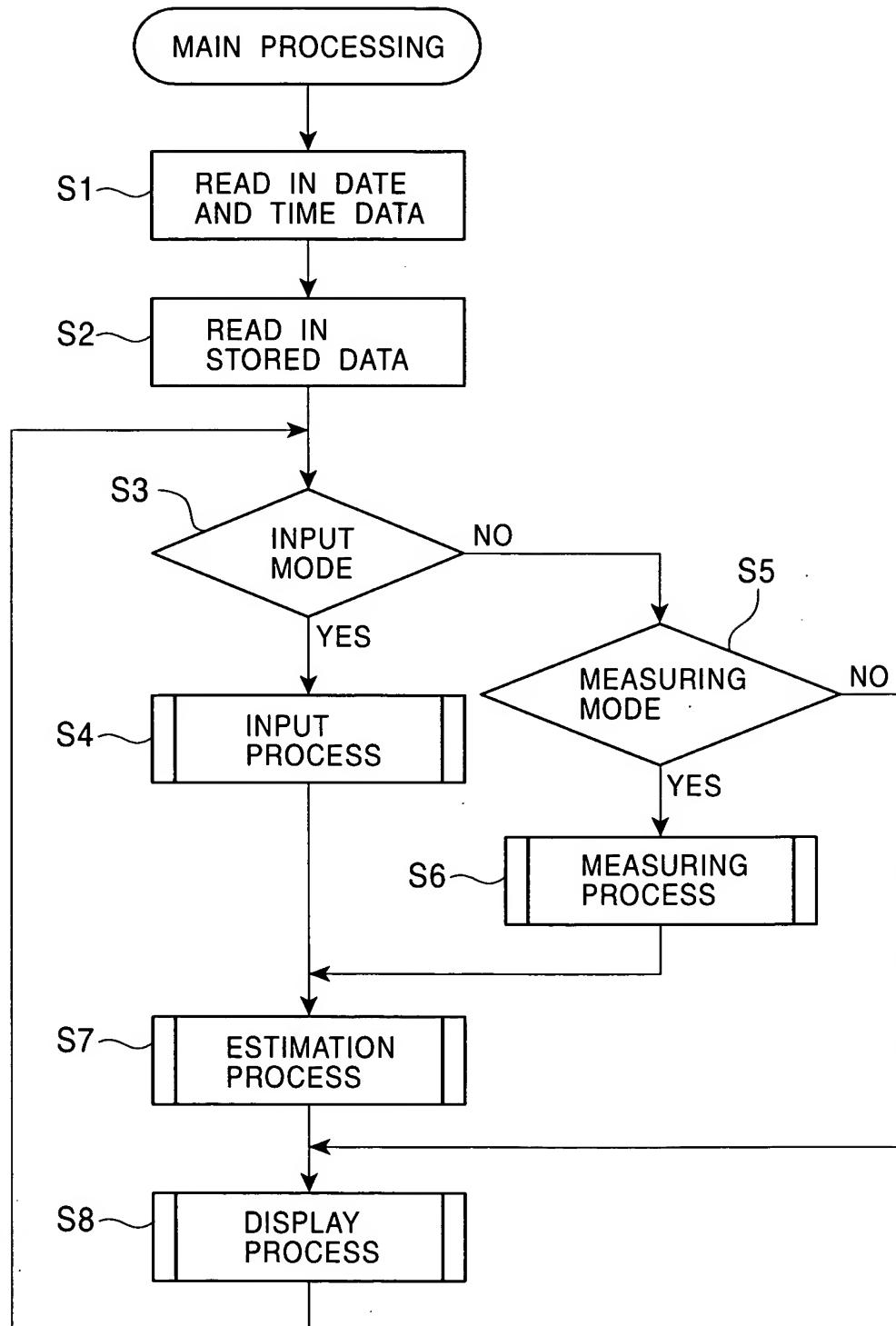


FIG. 4

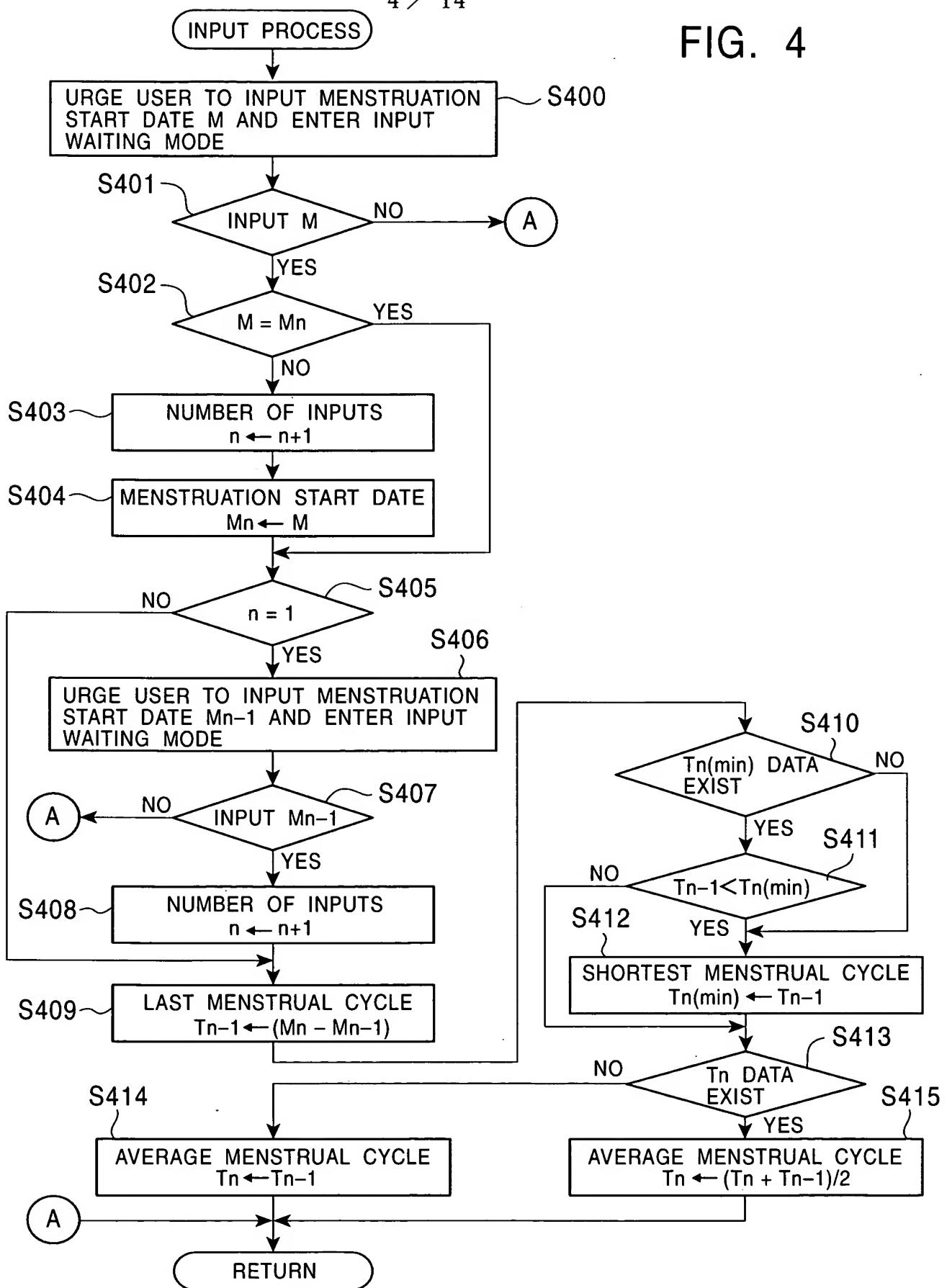


FIG. 5

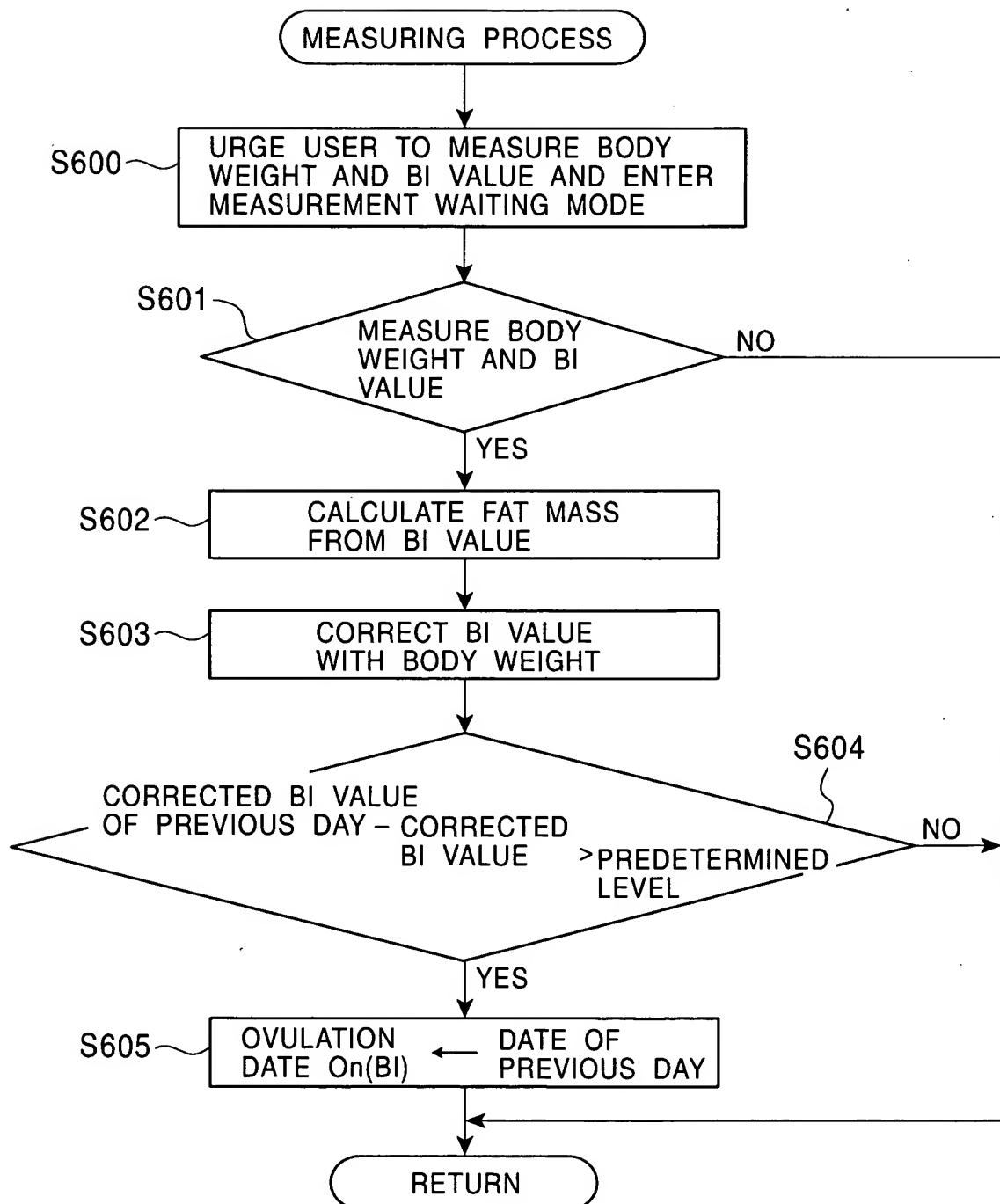


FIG. 6

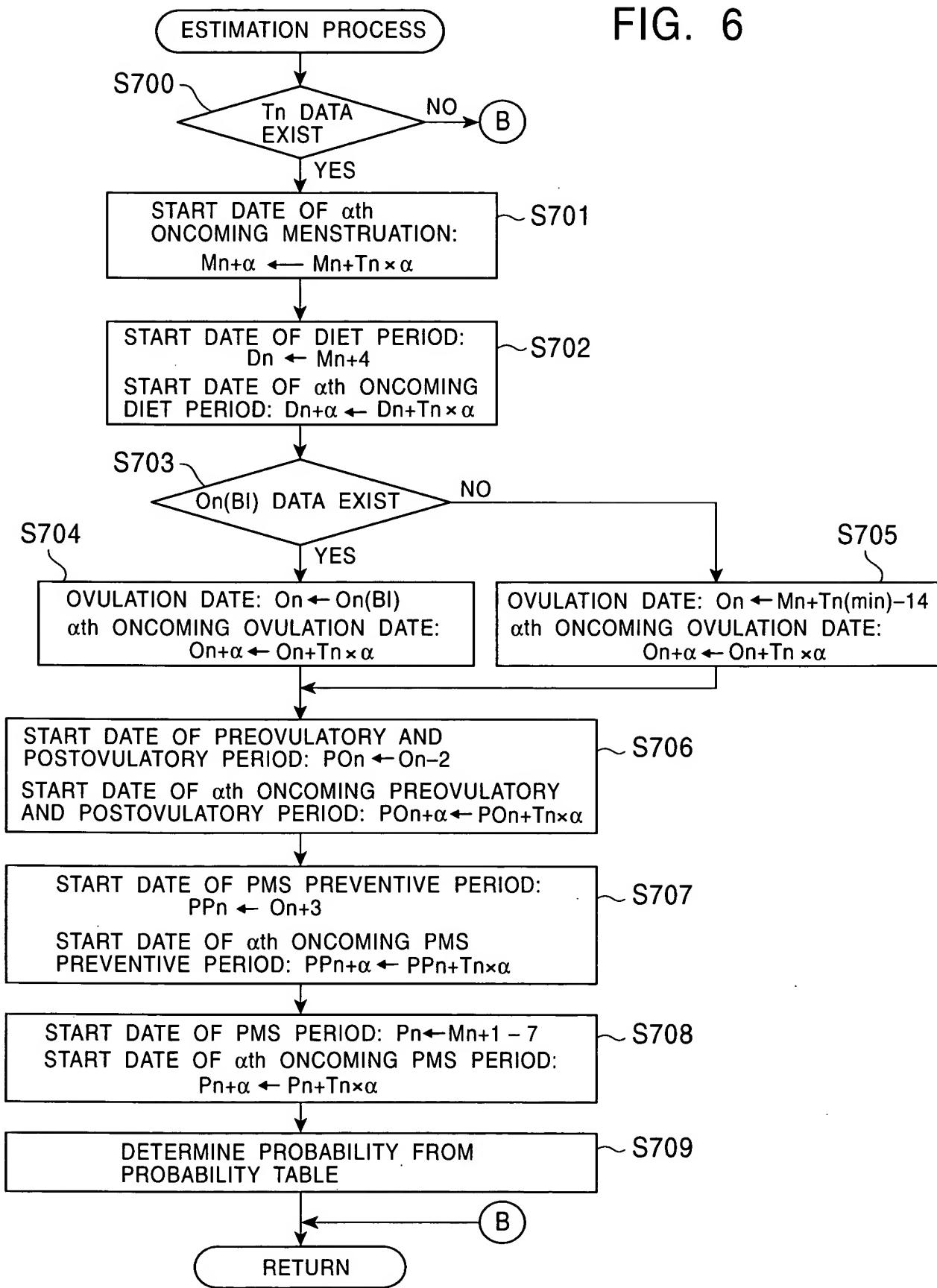


FIG. 7

NUMBER OF INPUTS n	PRESENT CYCLE	1st ONCOMING CYCLE	2nd ONCOMING CYCLE	3rd ONCOMING CYCLE	11th ONCOMING CYCLE	12th ONCOMING CYCLE
0 ~ 1	--	--	--	--	--	--	--
2 ~ 5	65%	50%	40%	30%	5%	5%
6 ~ 10	85%	75%	65%	50%	20%	15%
11 ~ 20	95%	85%	75%	65%	40%	35%
21 ~ 30	98%	95%	90%	75%	52%	48%
31 ~ 40	98%	98%	95%	90%	70%	65%

FIG. 8

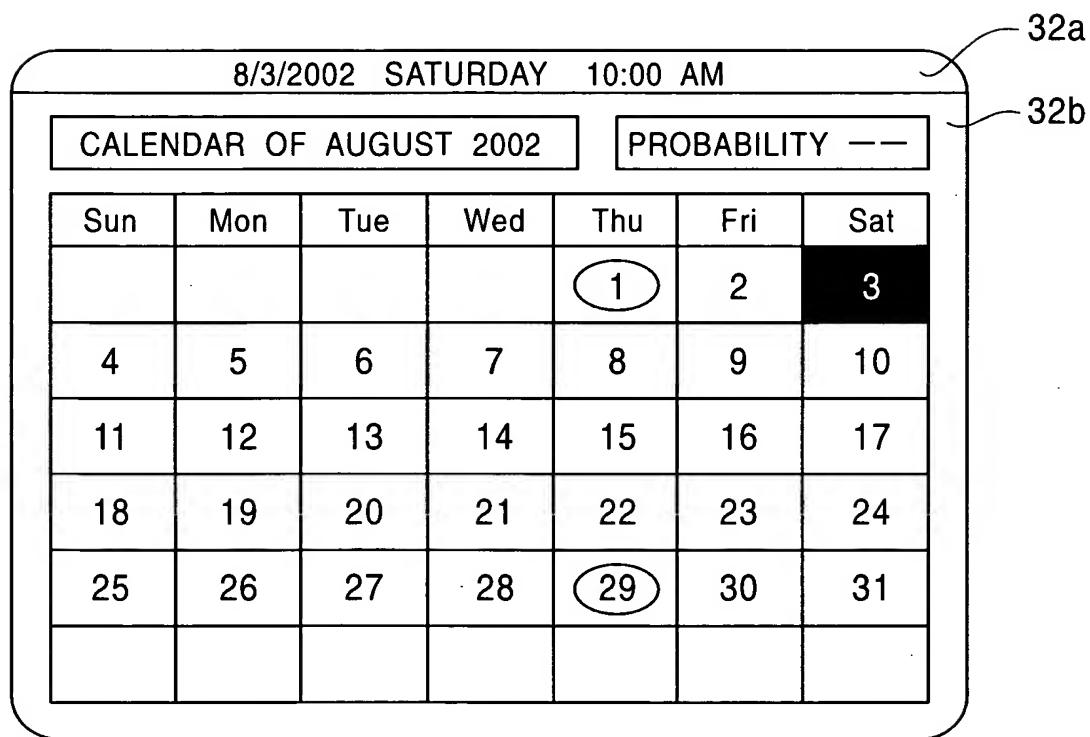


FIG. 9A

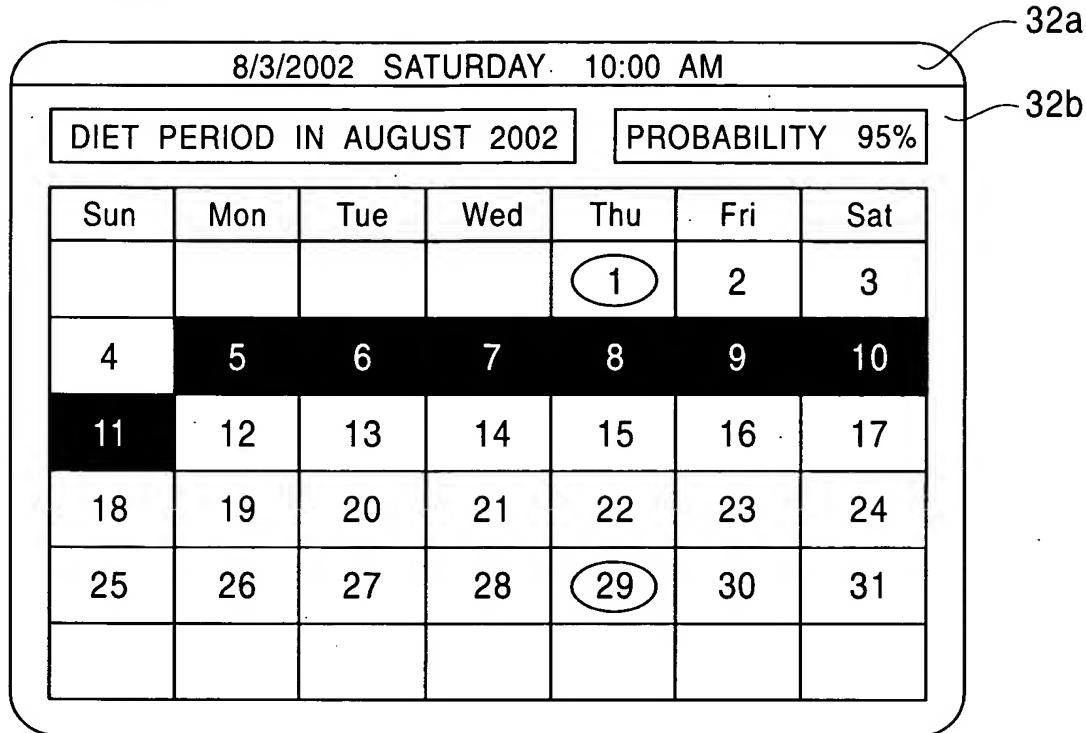


FIG. 9B

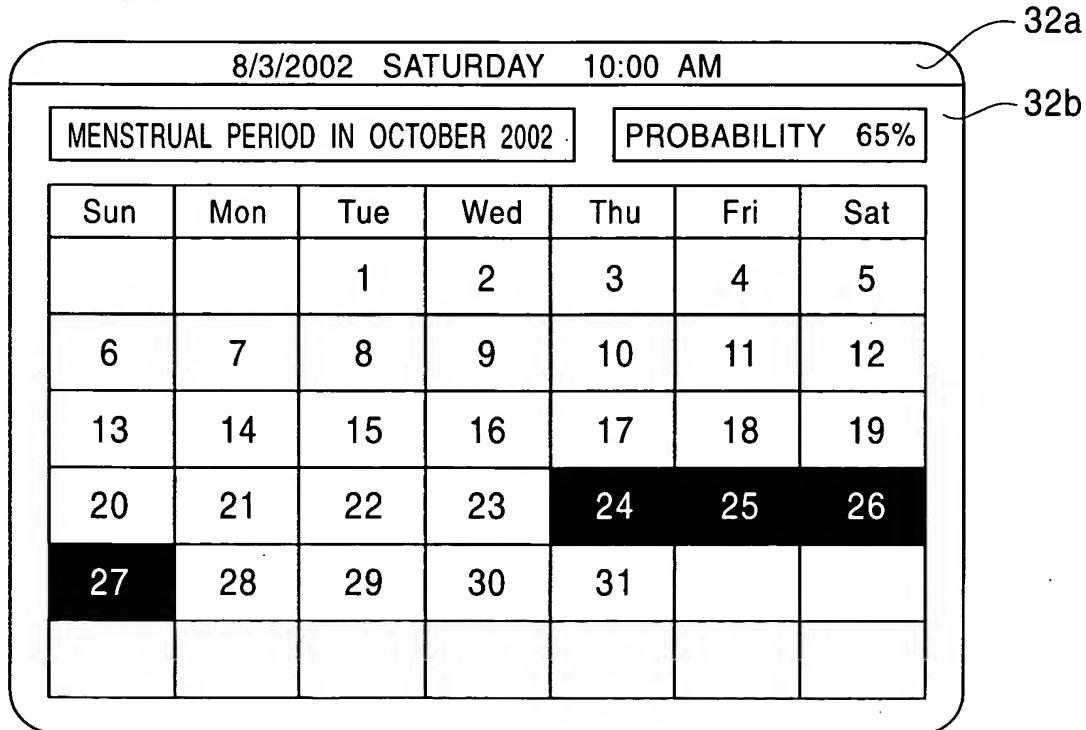


FIG. 10A

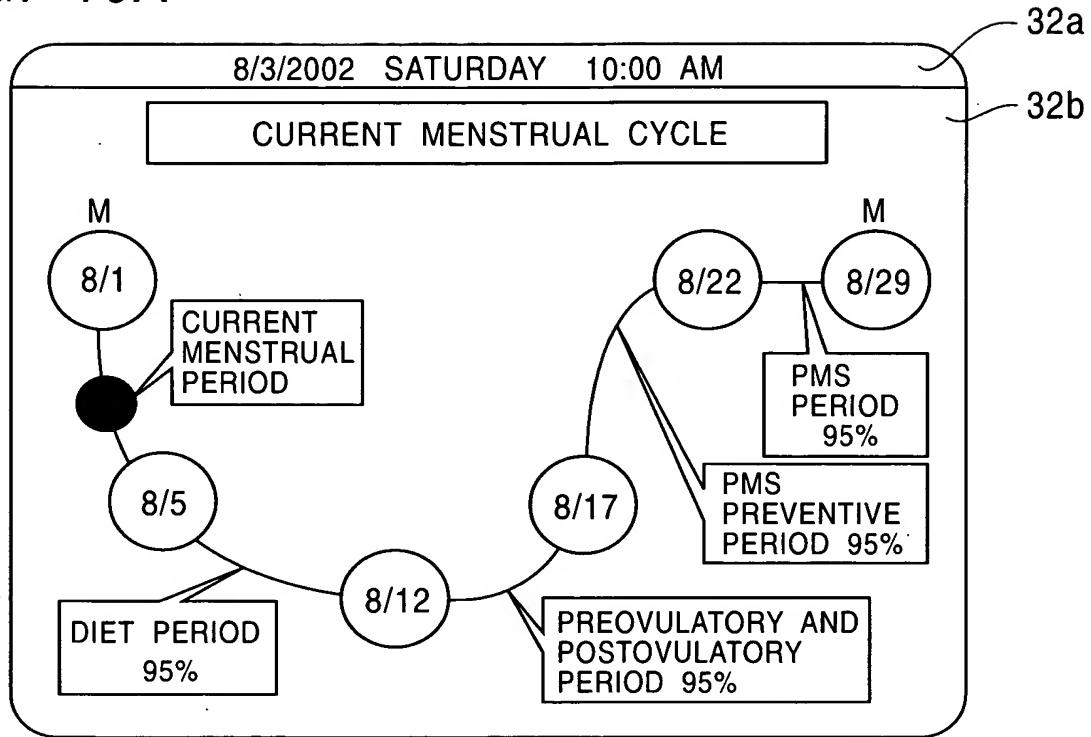


FIG. 10B

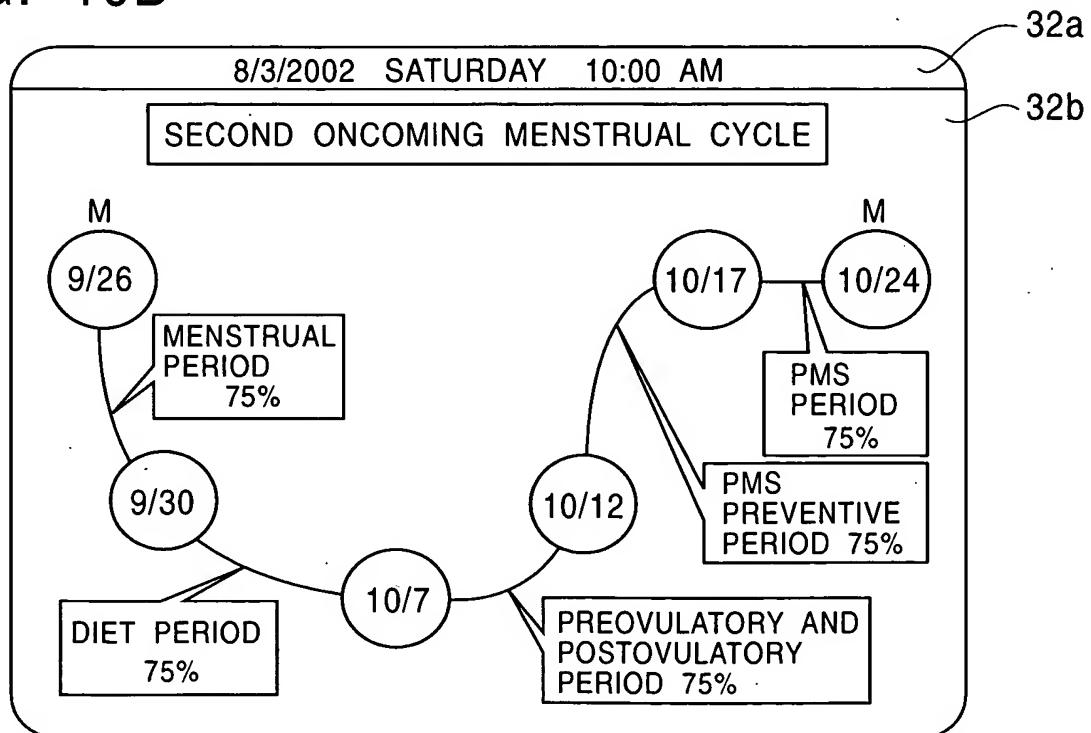
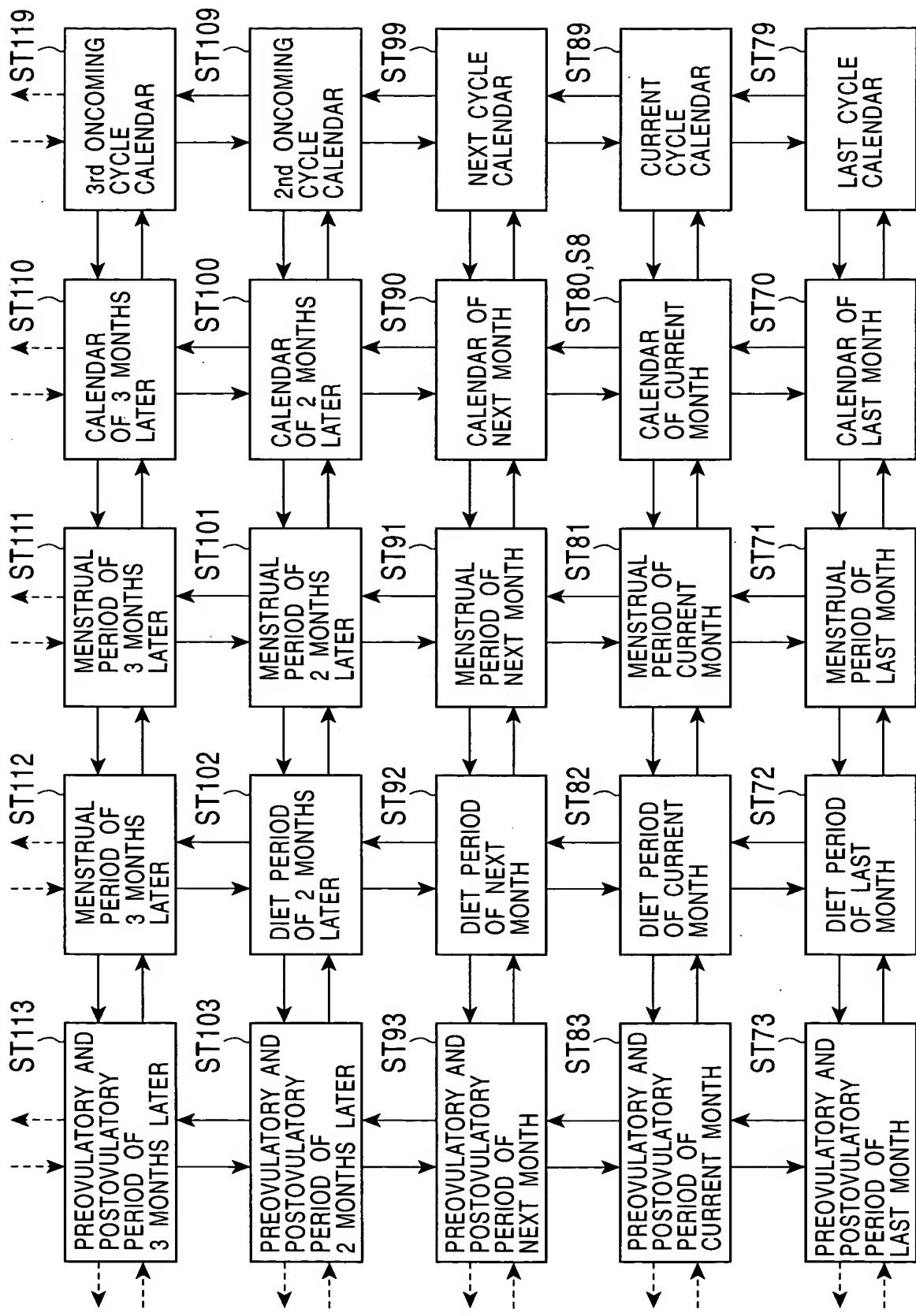


FIG.



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FIG. 12A

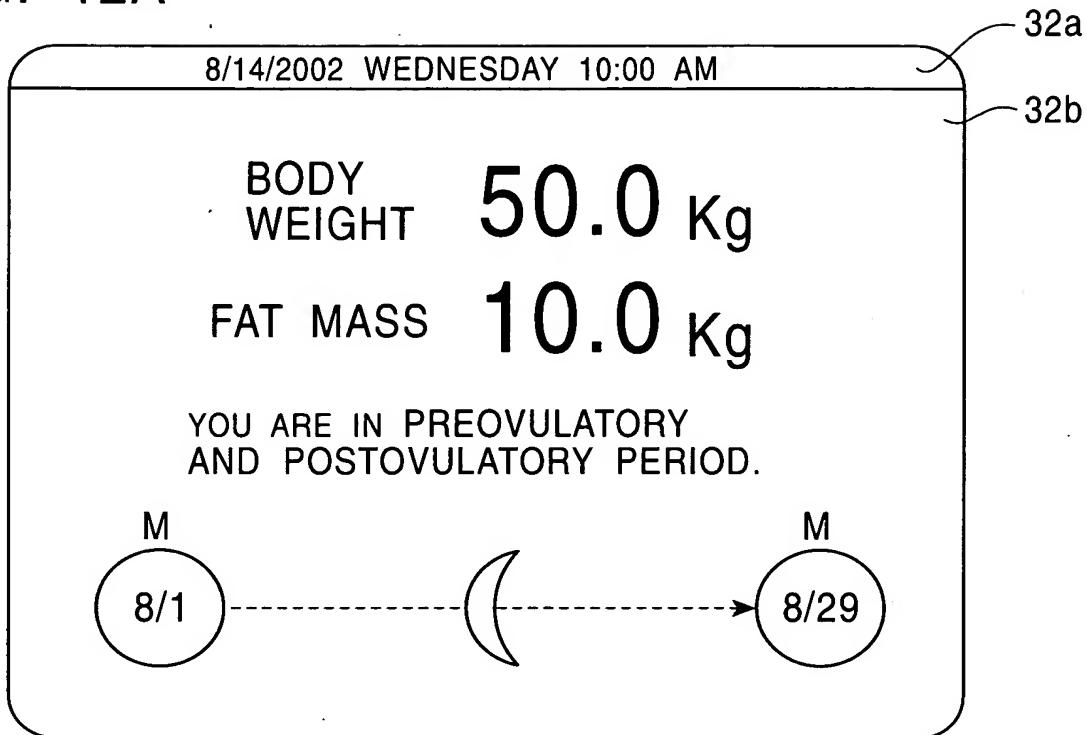


FIG. 12B

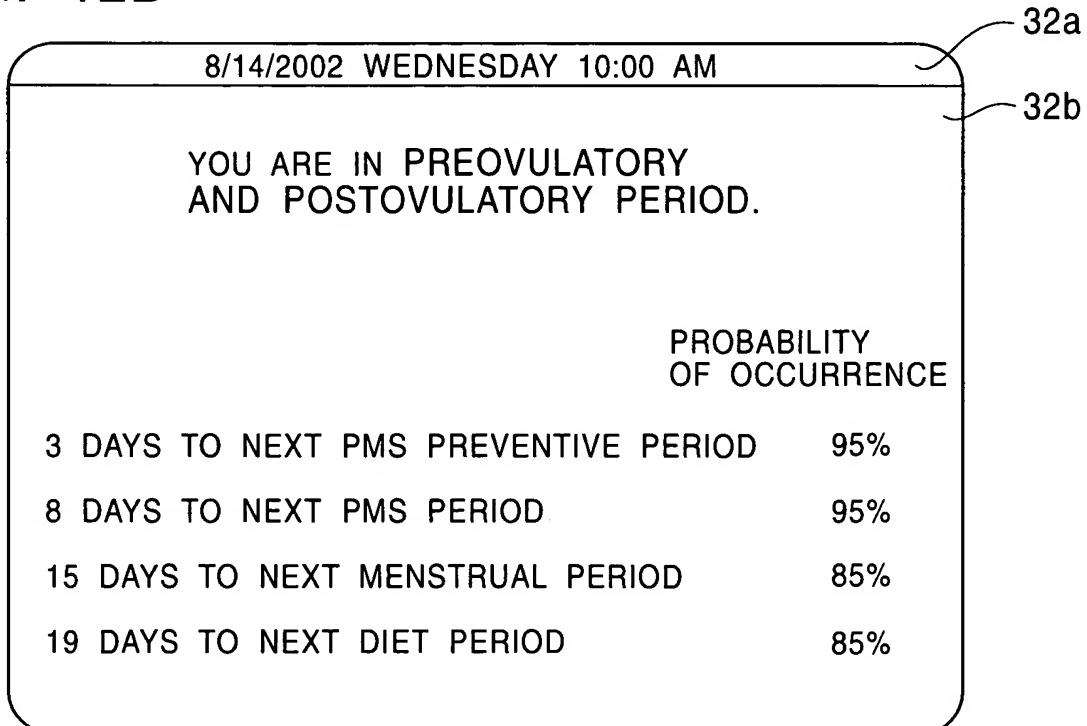


FIG. 13

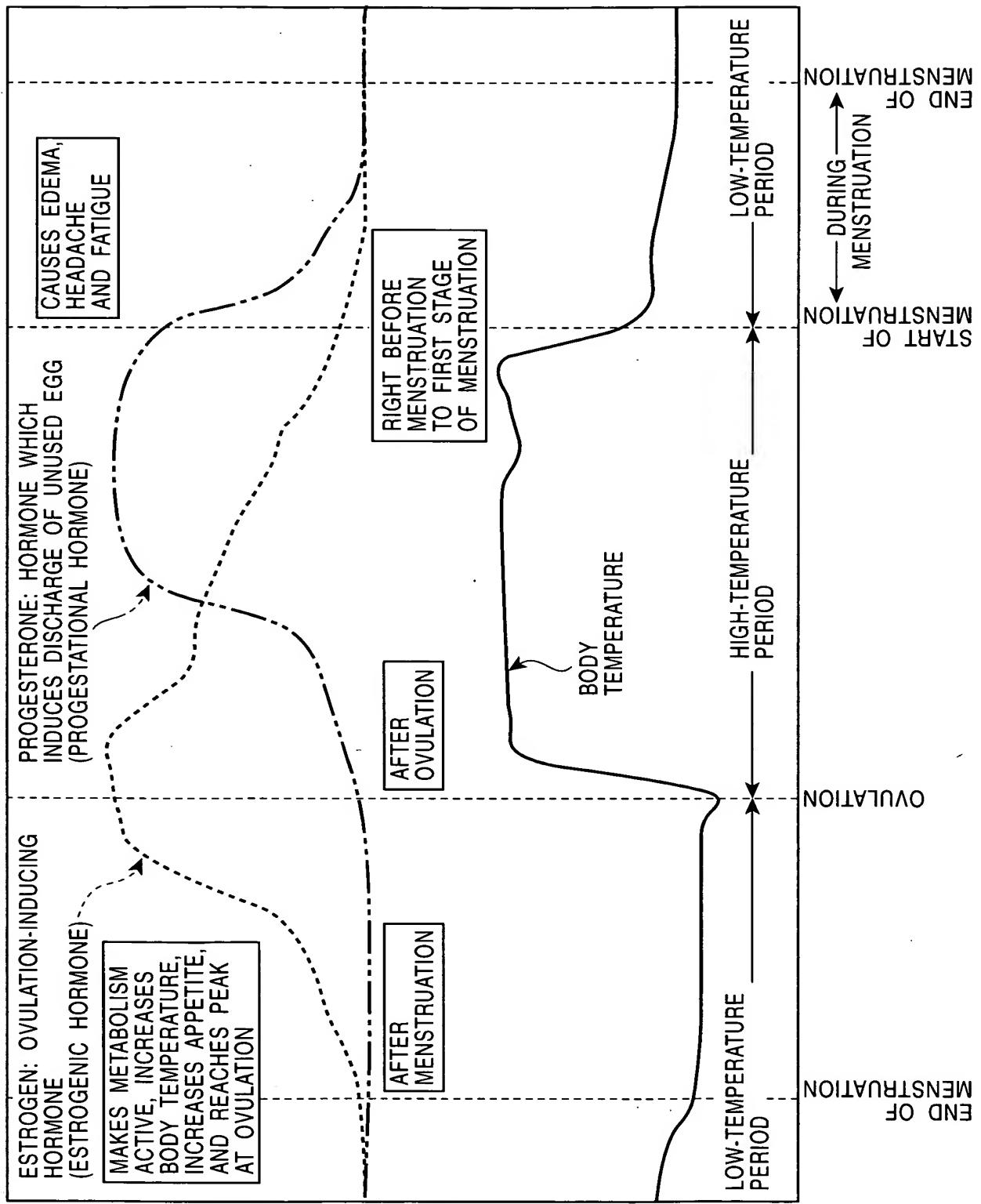


FIG. 14

